Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)	Atty. Docket No. NVIDP234/P000825	Application No.: 10/633,004
	Applicant: Singh et al.	
	Filing Date: 7/31/2003	Group Art Unit: Unassigned

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A						
	B						
	C						
	D						
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Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	V	Chou, Kuo-Yu et al., "Active Circuits Under Wire Bonding I/O Pads in 0.13 μm Eight-Level Cu Metal, FSG Low-K Inter-Metal Dielectric CMOS Technology +", October 2001, IEEE
	W	Efland, T., et al., "LeadFrameOnChip offers Integrated Power Bus and Bond over Active Circuit", 2001, International Symposium on Power Semiconductor Devices & ICs, Osaka
		Heinen, Gail et al., "Wire Bonds Over Active Circuits", 1994 IEEE

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.